Instrumentation Radar System

Subsystem Description/Summary and Description of CWBS Elements

FR Project No. 6904

Contract No. N60530-89-C-0067

Prepared for:

Naval Weapons Center
China Lake, CA

May 2, 1991

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LIST OF FIGURES

1.0 INSTRUMENTATION RADAR SYSTEM

The Instrumentation Radar System being developed at FR combines the features of an X-band radar tracker with a wideband, fully polarimetric coherent data collection system to enable the NWC to produce heretofore unachievable radar measurements on moving aircraft.

The proposed system features great versatility within the equipment complement, as well as the capability to accommodate future band upgrades. The salient features of the system being proposed by FR include:

- A full complement of antennas providing both narrowbeam and broadbeam coverage, optimized for tracking performance, polarization isolation, and channel-to-channel tracking
- Matched sets of monopulse comparators optimized for phase and amplitude tracking from unit to unit
- A fast gimbal featuring excellent dynamic tracking accuracy at high angular acceleration
- A high power transmitter subsystem capable of continuously optimized variable PRF
- Programmable waveform generation featuring frequency-polarization diversity and operator variable pulse width and prf sequencing
- An eight channel coherent receiver assembly featuring low noise RF circuitry housed adjacent to the antennas
- Selectable receiver IF bandwidths for optimum rise time/noise figure tradeoff, dual sample/hold amplifiers for fast acquisition/low droop, and microprocessor controlled AGC/STC
- A sophisticated microprocessor based range track processor that controls PRF, transmitter power, and antenna beamwidth
- A high speed tape drive and 80386 based workstation capable of recording rates exceeding 5 MB per second, with capability for channel playback and raw/corrected data plotting
- A video subsystem featuring a high grade commercial camera, Super VHS recorder, video annotator, and monitor
- A retrodirective, low coupling fixed calibration target

- A trailer assembly designed for minimum site set-up effort, complete with environmental control subsystem and electrical distribution system including appropriate line filtering, and lighting

- Fully documented and tested software based on internal software requirements specifications generated exclusively for the Instrumentation Radar application, implemented using standard FR and government procedures

Photos of the trailer exterior and interior are shown in Figure 1. A system block diagram is shown in Figure 2.

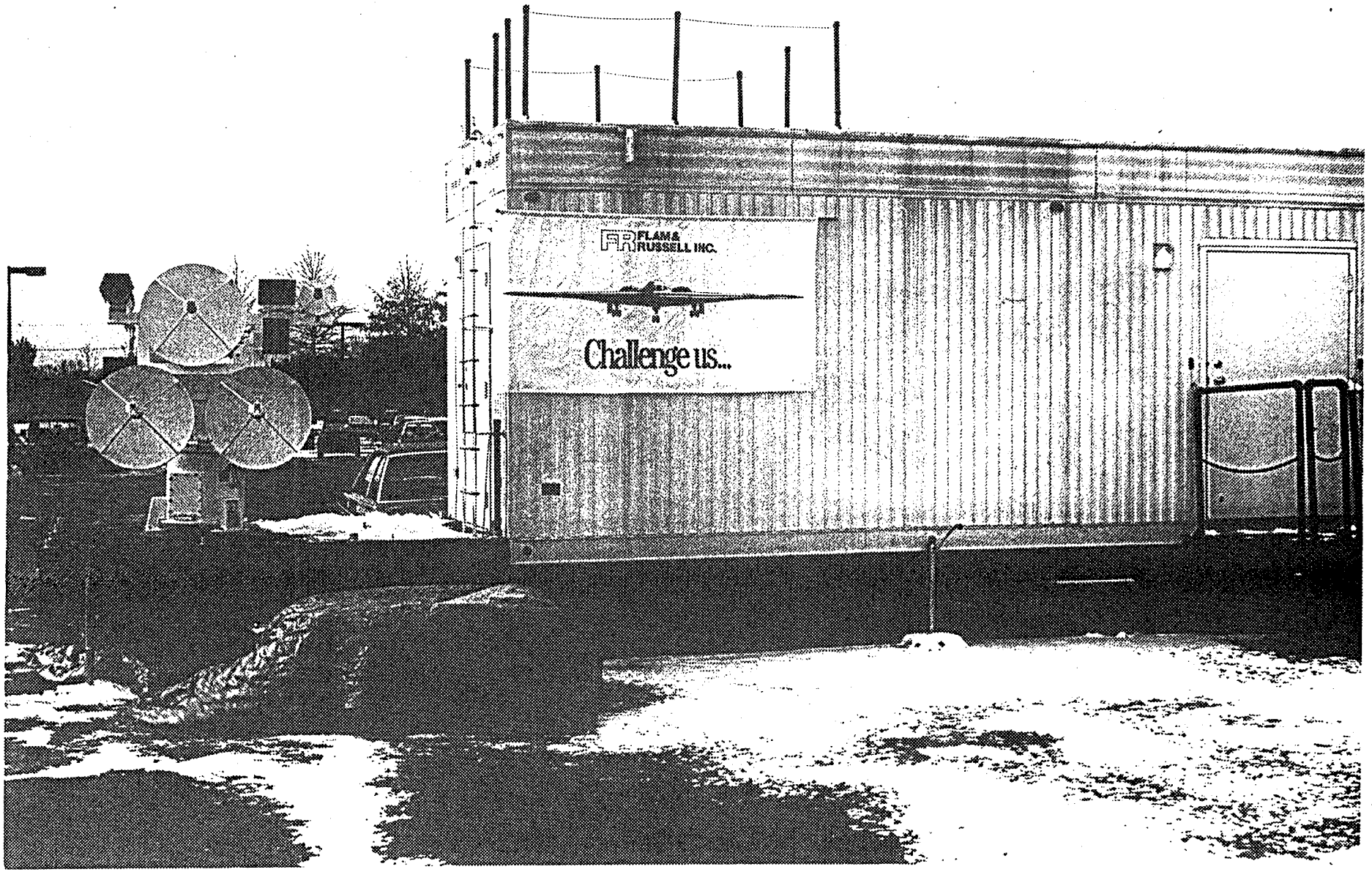


Figure 1. Instrumentation Radar System
(a) Exterior View

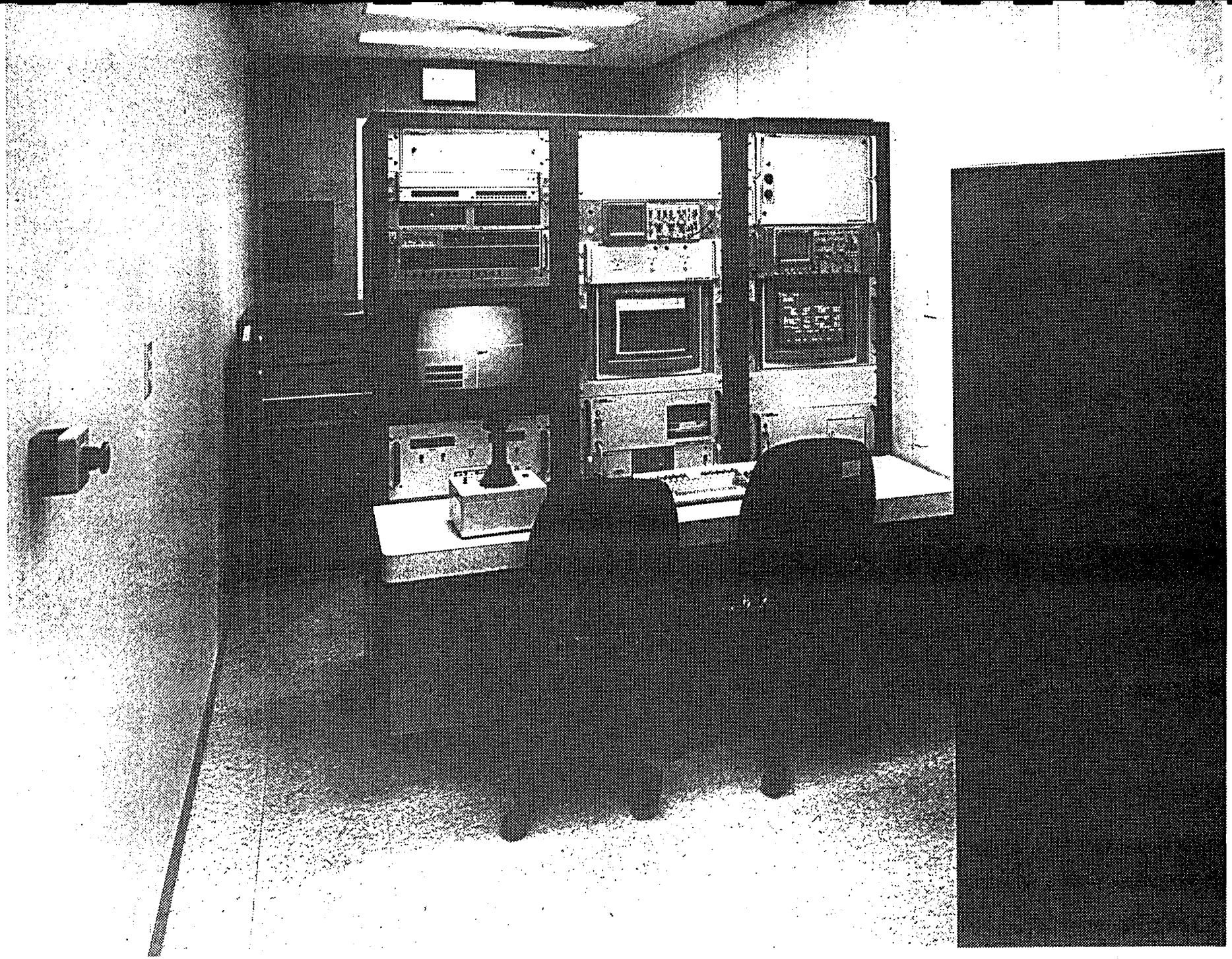
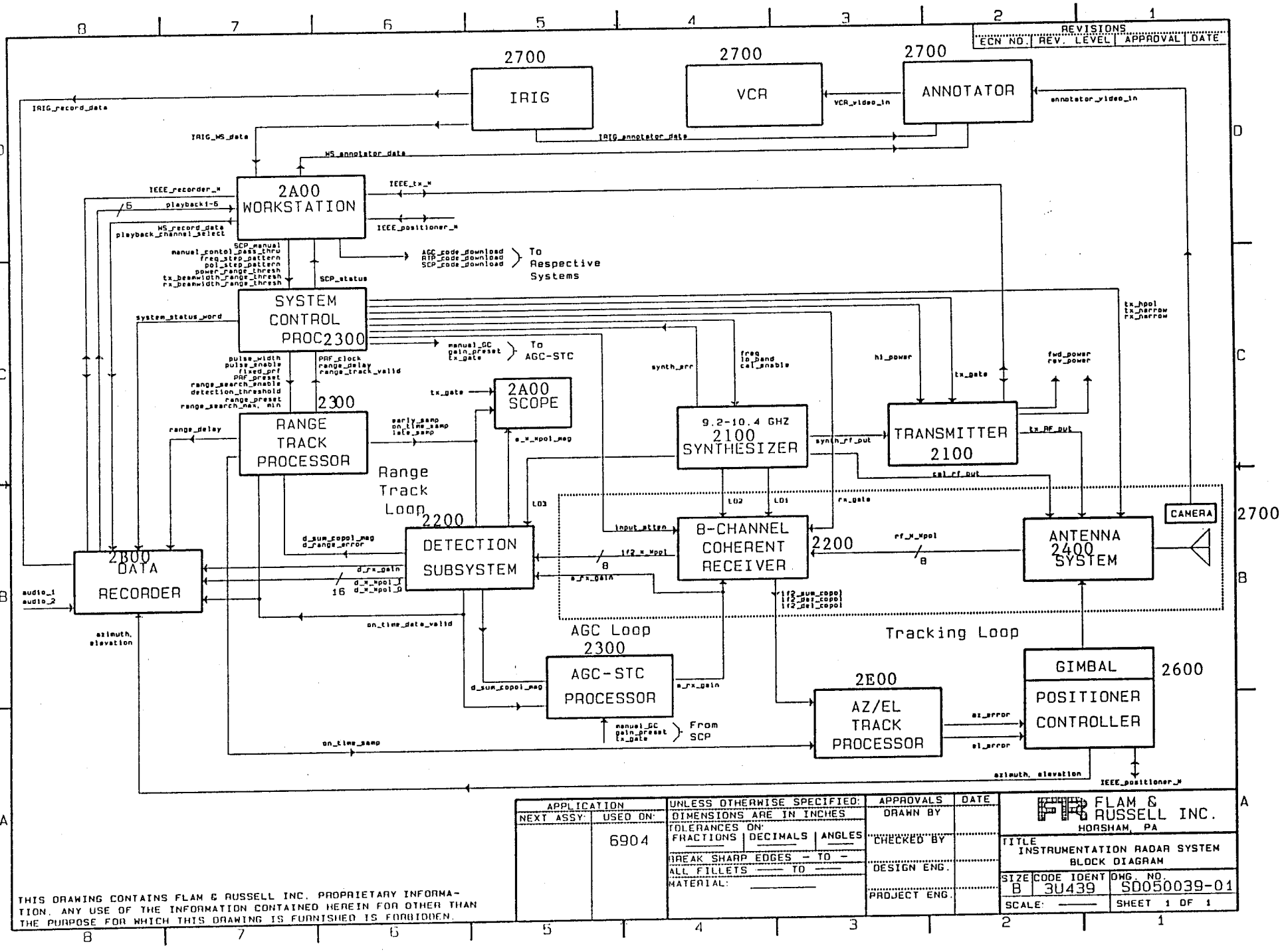


Figure 1. Instrumentation Radar System
(b) Interior View


REVISIONS
ECN NO. | REV. LEVEL | APPROVAL | DATE
2700
IRIG
2700
VCR
2700
ANNOTATOR
IRIG_record_data
IRIG_WS_data
IRIG_annotator_data
WS_annotator_data
VCR_video_in
annotator_video_in
2A00
WORKSTATION
IEEE_recorder_M
playback1-6
WS_record_data
playback_channel_select
IEEE_tx_M
IEEE_positioner_M
SCP_manual
manual_control_pass_thru
freq_step_pattern
pol_step_pattern
power_range_thresh
tx_beamwidth_range_thresh
rx_beamwidth_range_thresh
SCP_status
AGC_code_download
RTP_code_download
SCP_code_download
To Respective Systems
SYSTEM CONTROL PROC2300
system_status_word
manual_GC
gain_preset
tx_gate
To AGC-STC
pulse_width
pulse_enable
fixed_prf
PRF_preset
range_search_enable
detection_threshold
range_preset
range_search_max, min
PRF_clock
range_delay
range_track_valid
2300
RANGE TRACK PROCESSOR
range_delay
early_samp
on_time_samp
late_samp
tx_gate
2A00
SCOPE
e_M_hpol_mag
Range Track Loop
synth_src
freq_lo_band
cal_enable
hi_power
tx_gate
fwd_power
rev_power
tx_hpol
tx_narrow
rx_narrow
9.2-10.4 GHZ
2100
SYNTHESIZER
synth_rf_out
TRANSMITTER
2100
tx_RF_out
cal_rf_out
LO3
LO2
LO1
rx_gate
CAMERA
2700
2200
DETECTION SUBSYSTEM
d_sum_coppol_mag
d_range_error
input_atten
8-CHANNEL COHERENT RECEIVER
2200
rf_M_hpol
8
ANTENNA
2400
SYSTEM
2800
DATA RECORDER
audio_1
audio_2
azimuth,
elevation
d_rx_gain
d_M_hpol_I
d_M_hpol_Q
16
8
if2_M_hpol
e_rx_gain
if2_sum_copol
if2_del_copol
if2_del_copol
on_time_data_valid
AGC Loop
2300
AGC-STC PROCESSOR
d_sum_coppol_mag
e_rx_gain
Tracking Loop
2E00
AZ/EL TRACK PROCESSOR
manual_GC
gain_preset
tx_gate
From SCP
on_time_samp
az_error
el_error
GIMBAL
POSITIONER CONTROLLER
2600
azimuth, elevation
IEEE_positioner_M
APPLICATION
NEXT ASSY:
USED ON:
6904
UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS | DECIMALS | ANGLES
BREAK SHARP EDGES — TO —
ALL FILLETS — TO —
MATERIAL:
APPROVALS
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PROJECT ENG.
FLAM & RUSSELL INC.
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1000 System Engineering
This is the summary level for the effort to configure the IRS, determine system performance requirements, conduct system parameter simulations and trade-off studies, allocate requirements to specific subsystems, and to maintain interface control. All of these efforts have been completed, with the exception of interface control, which will continue to be maintained until the equipment ships. Upon completion of the above subtasks, some additional subtasks were added to the system engineering WBS item, and these follow.

1100 Interface Control
Update Interface Control Document as required during system integration and testing to reflect current system status.

1200 Close AGC Loop
Task completed. The AGC loop was tested while a full single channel of the receiver was integrated together over the full range of input levels.

1300 Close Range Track Loop
Task completed. A bench test setup was devised to simulate range movement in pulses injected into a fully integrated receiver channel, and the operation of the range tracking capability was demonstrated.

1400 Close Dynamic Tracking Loop
Perform closed loop test of angle tracking capability, demonstrating the use of receiver hardware, the AZ/EL preprocessor, and positioning subsystem hardware in the loop together. The positioning system angle tracking capability has been tested and is functioning properly. This exercise is a prelude to the system level tests described in the ATP summary.

2000 Hardware
This is the summary WBS level for the efforts to specify, design, procure, fabricate, assemble, integrate, and test all of the hardware subsystems described below.

2.0 TRANSMITTER SUBSYSTEM: TRANSMITTER

The Transmitter Subsystem provides the radar pulse to the antenna. In particular, it performs the following functions:

- It pulse modulates the RF carrier from the Synthesizer/LO Subsystem and amplifies the resulting pulsed RF signal to either 20 Watts (Low Power) or 4 Kilowatts (High Power).

- It diverts a small amount of the transmitted RF power to a power detector and A/D converter for forward power monitoring. This information goes to the Data Recorder.

The transmitter subsystem consists of two commercial TWTAs and associated pulse modulator, amplifier selection, and power monitor circuitry mounted in a separate RFI air cooled rack. The subsystem receives a 1 milliwatt CW signal at the transmit frequency from the synthesizer/LO subsystem. The signal is amplified, pulse modulated, and routed to the appropriate TWTA. The selected TWTA amplifies the signal pulses to nominal levels of 20 watts or 4000 watts, respectively. The TWTA outputs run to an electromechanical waveguide transfer switch which routes the appropriate output to the antenna line (TX_RF_OUT) while the other output is terminated.

The 4000 watt TWTA unit contains a solid state amplifier and a travelling wave tube that is beam or cathode modulated. The electron beam is turned off during the quiescent state and when the receiver RF gate is closed. The tube noise is eliminated to at least -90 dBc when the beam is turned off.

The 20 watt TWTA is a catalog item which uses a CW rated travelling wave tube as the amplifier element. A 20 watt PIN diode switch is used at its output to eliminate tube noise when an RF input pulse is not present. The RF power level at the switch output is 16 watts.

The transmitter subsystem has a forward power detector which sends digital data to the data recorder. The RF signal is sampled, AM detected and converted to 8 bits of latched data. The detected signal is sampled 80 nsec. after the RF pulse rise time (TXRF_GATE). At the end of conversion, the data is latched onto the data bus, D_FWD_POWER by the latching signal, DATA_CLOCK. The detector has 10 dB of range, set between +4 and -6 dB of nominal. Nominal power is either 16 watts or 4000 watts, depending upon the setting of HI_POWER.

A block diagram of the transmitter subsystem is shown in Figure 3.

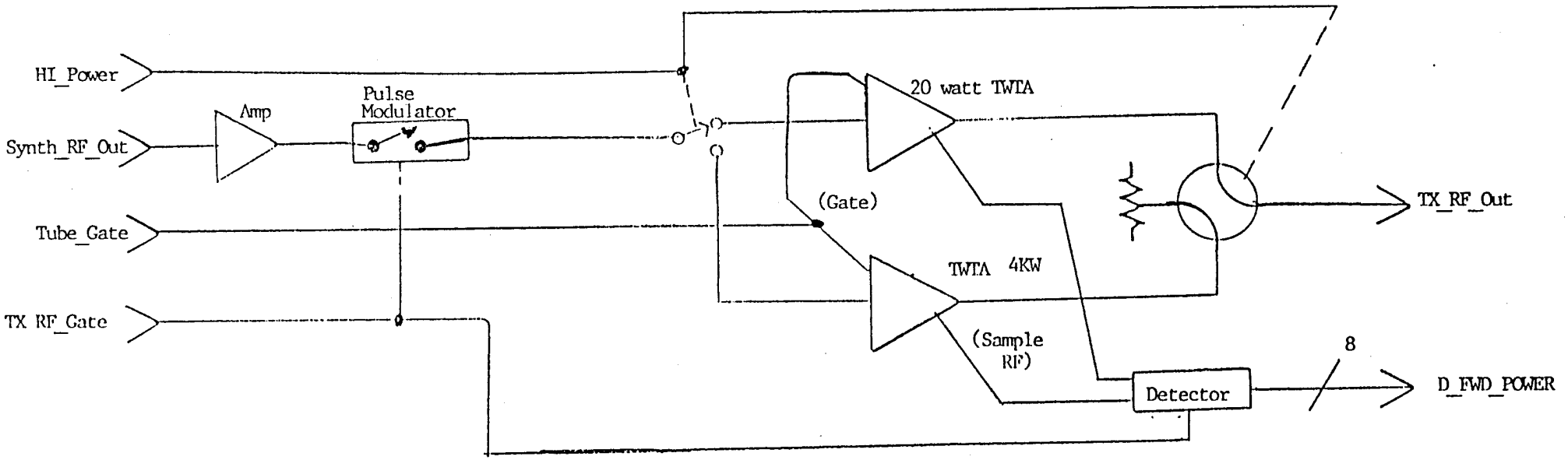

Fig. 3. Transmitter Block Diagram

3.0 TRANSMITTER SUBSYTSEM: SYNTHESIZER/LO

The Synthesizer/LO provides the RF carrier, all the Local Oscillator carriers, and the RF calibration signal used by the radar. In particular, it performs the following functions:

- It sends a stepped frequency carrier from 9.2 to 10.4 GHz to the Transmitter Subsystem for the main radar signal.
- It sends a stepped frequency first LO signal (LO-1) in the 5.55 to 6.75 GHz range to the 8-Channel Coherent Receiver for the first downconversion.
- It sends a fixed frequency second LO signal (LO-2) at 3.35 GHz to the 8-Channel Coherent Receiver for the second downconversion.
- It sends a fixed frequency third LO signal (LO-3) at 300 MHz to the Detection Subsystem for downconversion to baseband.
- It provides a stepped frequency carrier from 9.2 to 10.4 GHz for calibration of the 8-Channel Coherent Receiver.
- It provides a 10 MHz crystal reference signal to synchronize other timing circuits in the radar.

The synthesizer subsystem consists of a commercial 1 to 2 GHz synthesized signal generator and associated frequency conversion and switching circuitry enclosed in a rack mount assembly. The Sciteq generator accepts a 10 MHz reference signal and a 35 bit binary frequency control word, and generates a +10 dBm carrier between 1 and 2 GHz. It has a frequency switching speed of 750 nsec and direct digital synthesis within 25 MHz segments.

The FR assembly contains a 10 MHz reference oscillator and four phase locked oscillators, along with couplers, filters and amplifiers. It generates RF carriers for the three local oscillator signals, transmitter, and calibration circuit. All carriers are phase locked to the reference and therefore are coherent to each other. If any oscillator is out of lock, the RF signal from the Sciteq synthesizer is gated off and the SYN_ERROR alarm is activated. The LOW_BAND input selects either the 9.2 to 10.2 GHz band or the 9.4 to 10.4 GHz band by switching one of two oscillators to mix with the Sciteq generator. These oscillators produce outputs at 8.2 and 8.4 GHz respectively, and are energized all the time (but sufficiently isolated when not selected). A set of RF switches routes the proper oscillator output to the mixer. The mixer output is filtered and used to drive the transmit subsystem. The calibration signal is sampled here, amplified and

run to a gate switch, controlled by CAL_ENABLE. A programmable attenuator, controlled by the digital signal CAL_ATTN, sets the signal to one of 62 power levels before it runs to the 16 way calibration splitter as signal CAL_RF_OUT.

LO 2 and LO 3 are generated by two phase locked oscillators, at 3350 MHz and 300 MHz respectively. These signals are amplified and routed to the receiver and detector subsystems.

LO 1 is generated by first mixing the carriers of the LO 2 and LO 3 oscillators to produce a 3650 MHz signal. It is filtered and mixed with a sampled transmit signal at 9.2 to 10.4 GHz to produce a 5.55 to 6.75 GHz signal. This is filtered, amplified and sent to the coherent receiver as LO 1. LO 1 is therefore the transmit frequency with a 3.65 GHz offset, and LO 2 and LO 3 are fixed frequency carriers.

A simplified block diagram of the synthesizer is shown in Figure 4.

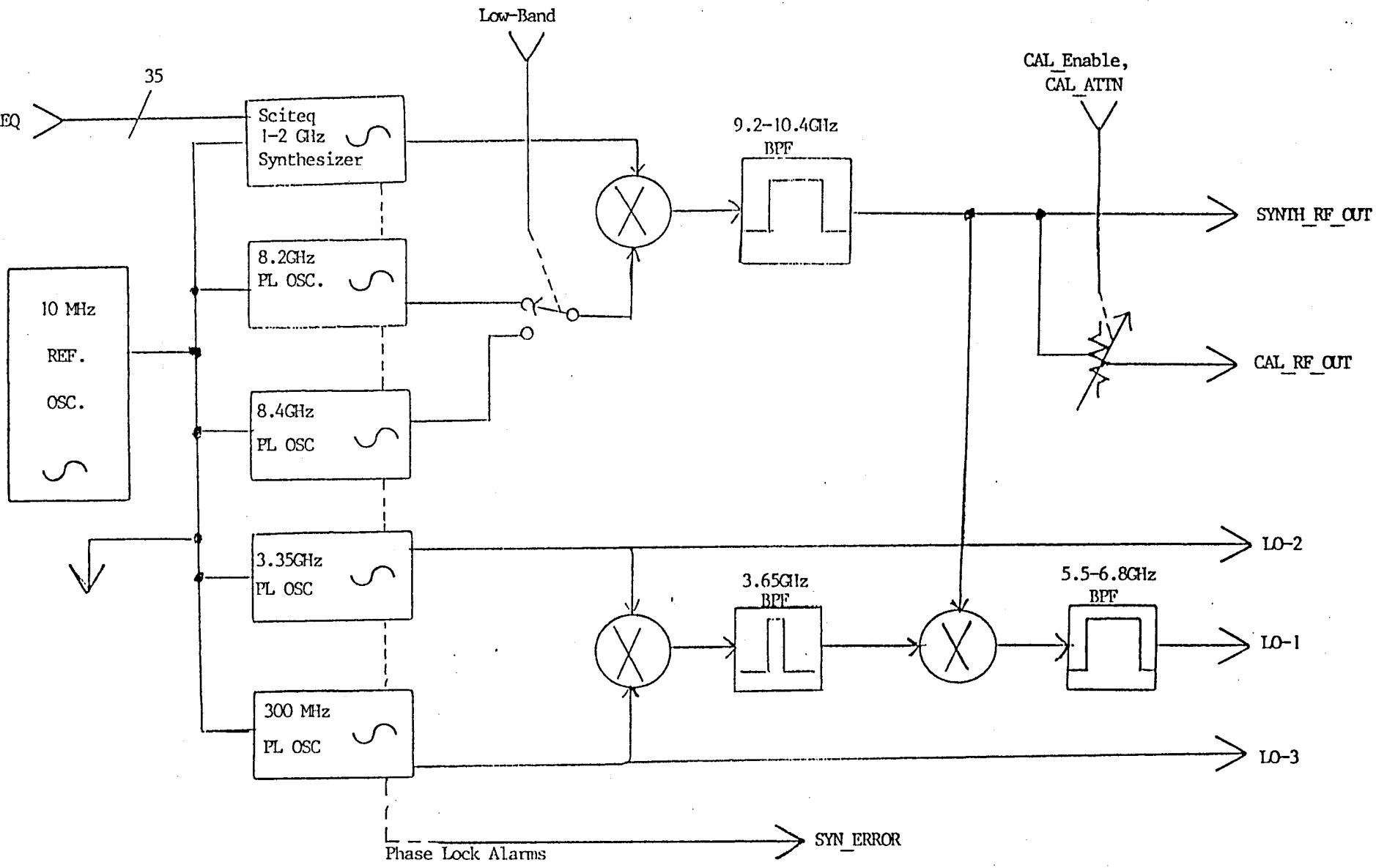

Fig. 4. Synthesizer Block Diagram

2100 Transmitter Subsystem
This is the summary level WBS for the efforts involved in specifying, designing, procuring, fabricating, assembling, and testing the transmitter subsystem, which includes the high and low power TWTA's, the synthesizer, the transmitter exciter assembly, and the switch box.

2110 Synthesizer Box Assembly & Test
Task completed. The synthesizer was tested for resolution and accuracy of the output RF and LO frequencies, output power levels, harmonics and spurious products.

2120 Transmit Exciter Box Assembly & Test;
Forward Power Board Checkout. Complete wiring of transmitter exciter box assembly and test pulse formation characteristics. Test detector level inputs into forward power A/D board and analog/digital outputs.

2130 Switch Box Assembly and Test
Task completed. The box was tested for proper functionality.

2140 Power Supply Assembly and Test
Task completed. The assembly was tested for rated power under load.

2150 Rack & Cable Transmitter Subsystem
Permanently mount exciter and amplifiers in transmitter rack assembly and interconnect units; run waveguide to interconnect with antenna subsystem. The exciter and amplifiers are in the rack assembly currently, but are not permanently mounted. The essential elements of the unit have been integrated and tested for functionality and proper pulse shapes and characteristics.

2160 Receive and Check High Power Amplifiers
Task completed. The amplifiers have been tested for rated power and pulse characteristics. The units underwent testing to an approved ATP at the vendor facilities.

2170 Integrate and Test Transmitter Subsystem;
Check Interface with Workstation. Check operation of integrated transmitter subsystem per ATP summary (including synthesizer tests). Check workstation control/status monitoring of amplifiers.

4.0 RECEIVER SUBSYSTEM: EIGHT CHANNEL COHERENT RECEIVER

The Eight Channel Coherent Receiver takes the 8 received radar signals from the Antenna Subassembly (co-polarized and cross-polarized outputs from the 4 comparator outputs) and downconverts them to 300 MHz. In particular, it performs the following functions:

- It takes the inputs from both broadbeam and narrowbeam antennas, amplifies them to establish the noise figure, and selects one preamplifier output for downconversion.
- It performs a double conversion from the 9.2 - 10.4 GHz frequency range to a fixed frequency of 300 MHz.
- It bandlimits the received radar signal and rejects image and spurious frequency components.
- It gates out the transmitted pulse leakage and near-in clutter returns.
- During Calibration, it injects the 9.2 - 10.4 GHz calibration signal into its RF input in place of the inputs from the Antenna Subsystem.
- It attenuates returns from oversized radar targets on command from the System Control Processor.

The eight channel coherent receiver is an FR built assembly mounted on the pedestal, at the rear of the antennas. It is housed in a sealed, temperature controlled enclosure.

The receiver has eight channels, with two selectable inputs per channel from the broadbeam or narrowbeam antennas, or 16 total input ports. The calibration signal (CAL_RF_OUT) runs to the receiver enclosure, where it is split into 16 similar signals. They are coupled into the receiver input channels by semirigid cable to waveguide couplers mounted on the rear of the individual antennas. The 16 channels are routed to the receiver enclosure by waveguide where they go to 16 solid state limiters, and then to 16 low noise preamplifiers, though space is allocated to add preselector filters between the limiters and LNAs. Eight solid state transfer switches, controlled by the signal RX_NARROW, select eight channels from the desired antenna to be processed further.

Another set of solid state transfer switches select attenuators when needed for oversized radar targets. The signal is filtered, amplified, and then processed by an assembly of eight downconverter modules.

The receiver RF frequency range is 9.2 to 10.4 GHz, which is downconverted to a first IF of 3.65 GHz by a variable frequency (LO-1) of 5.55 to 6.75 GHz. The first IF is converted to a second IF of 300 MHz by a fixed 3.35 GHz carrier (LO-2). The block diagram of the receiver subsystem is shown in Figure 5.

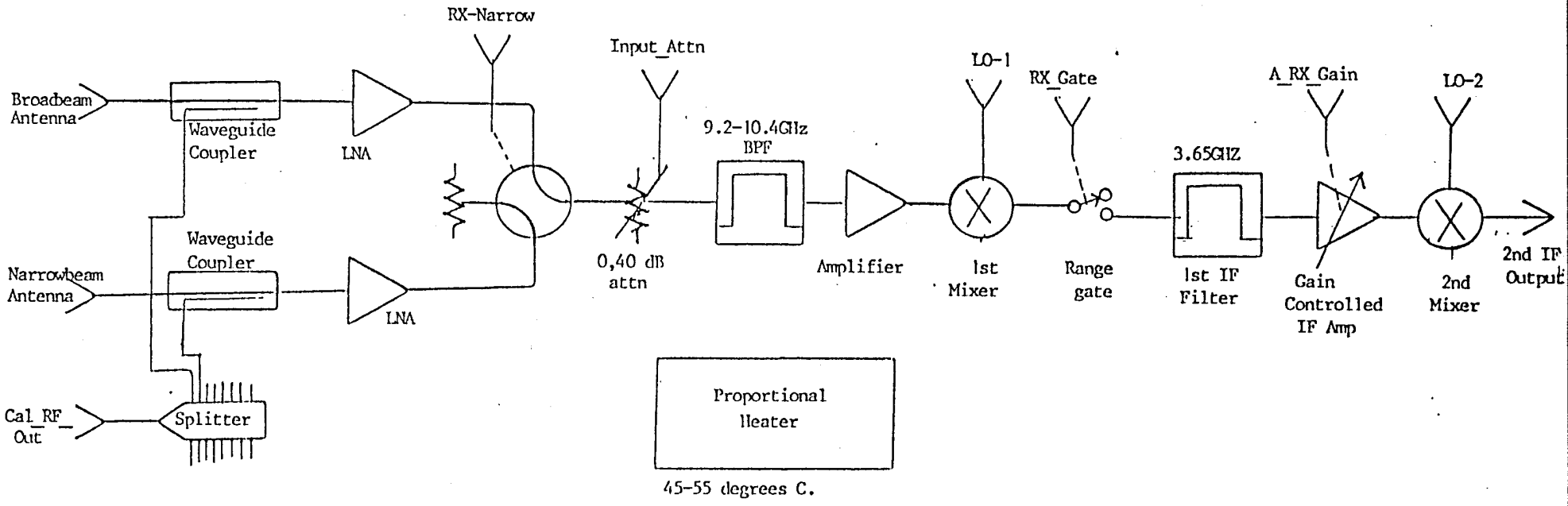

Fig. 5. 8 Channel Coherent Receiver Block Diagram

5.0 RECEIVER SUBSYSTEM: DETECTOR

The Detection Subsystem downconverts the 300 MHz 2nd IF signals to digital baseband and derives input signals to other subsystems from these signals. In particular, it performs the following functions:

- It converts all 8 of the 300 MHz 2nd IF radar returns to I and Q baseband voltages and digitizes them for input to the Data Recorder Subsystem.
- It converts the copolarized sum channel 300 MHz 2nd IF radar return to digitized I and Q Early and Late range samples for input to the Range Track Processor.
- It provides the copolarized sum, azimuth difference, and elevation difference signals at the 300 MHz 2nd IF to drive the AZ/EL Track Processor.
- It provides 8 pairs of I and Q baseband analog radar returns to be displayed on the Oscilloscope Subsystem.

A block diagram of the detection subsystem is shown in Figure 6.

The detection subsystem converts the eight 300 MHz IF2 signals (from the 8-channel coherent receiver) to I/Q baseband signals. The baseband signals are applied to sample/hold amplifiers which sample the target return radar pulses at the middle of the pulses (on-time sample). There are two additional pairs of sample/hold amplifiers which sample one I/Q baseband signal pair (signals derived from if2_sum_copol) on its rising edge (early sample) and on its falling edge (late sample).

The sampled signals are A/D converted into 8-bit digital signals. All of the on-time digital signals go to the data recorder. The on-time digital copol and xpol sum signals also go to the AGC-STC processor. The early, on-time, and late digital copol sum signals go to the range track processor.

All eight channels are ganged gain controlled before the down conversion to baseband. The gain control works to keep the maximum of the copol and xpol sum signal at a constant level.

There are two other sets of outputs. One is eight pairs of I/Q analog baseband signals; these are used for the A-scope displays. The other is a set of three co-polarized 300 MHz IF signals coupled off just before the down conversion; these are used for the AZ/EL track processor.

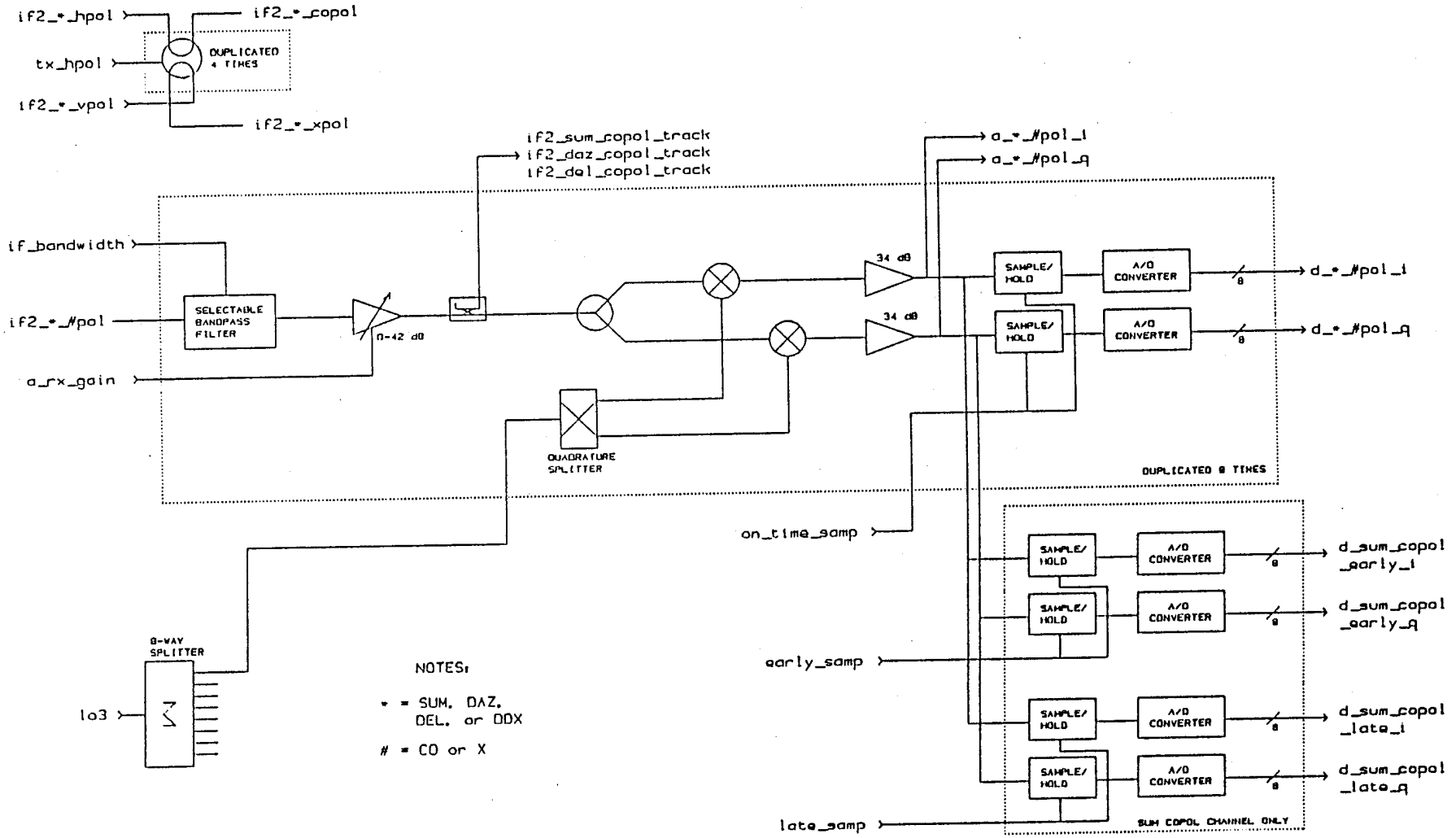

Fig. 6. Detection Subsystem Block Diagram

2200 Receiver Subsystem
This is the summary level WBS for the efforts to specify, design, procure, fabricate, assemble, and test the receiver subsystem, including an eight-channel coherent receiver assembly, a detector assembly, and a receiver heater box.

2210 Rx Front Ends Assembly & Test
Task completed. All eight of the receiver front end plates have been assembled and tested for gain, noise figure, and relative phase/amplitude tracking performance.

2220 Coherent Rx Enclosure Assembly & Test; Mount Enclosure on Antenna Frame
Test receiver front end assemblies when mounted in weather-proof enclosure and configured with final interconnection cabling. Mount unit on antenna positioner.

2230 Heater Enclosure Assembly & Test; Mount Enclosure on Antenna Frame
Assemble receiver proportional temperature controller into weatherproof enclosure and mount on antenna positioner. Check heater box operation in final configuration.

2240 Material Procurement
Task Completed.

2250 Detector Board Tests
Task completed. The detector board tests included checkout of the control board, all ten A/D boards including full bit checks, four transfer switch boards, four downconverter boards, and four bandpass filter boards.

2260 Detector Enclosure Assembly & Test
Task completed.

2270 Rack & Cable Detector Assembly
Task completed.

2280 Integrate & Test Receiver Subsystem
Interconnect receiver elements in final physical configurations (e.g., interconnect 8 channel coherent receiver enclosure on pedestal to Detector enclosure inside trailer in conjunction with task 2470) and perform integrated receiver tests per the ATP summary.

6.0 AUXILIARY PROCESSORS: SYSTEM CONTROL PROCESSOR

The System Control Processor (SCP) performs the following functions:

- It acts as a high-speed real-time control intermediary for the Workstation.
- It receives high level commands from the Workstation through an RS-232 serial interface; through the SCP, the workstation can control all three auxiliary processors.
- It generates the global timing signals for the radar.
- It performs range threshold monitoring and frequency/ polarization sequencing.

The System Control Processor (SCP) in an intermediate level controller implemented as a C language program running in the 80386/7 Auxiliary Processor hardware. The SCP, making use of some special purpose digital circuitry, acts as a high speed control intermediary for the Workstation. The purpose of the SCP is to handle the real-time control tasks that would overly burden the Workstation. Tasks such as range threshold monitoring and frequency/polarization sequencing cannot be reliably performed by the Workstation as it responds to asynchronous interrupts. The SCP runs in hardware that is isolated and specially dedicated to the task of high speed control.

High level commands from the Workstation are received through ws_scp_data, an RS-232 serial interface (4800,E,7,1). These ASCII sequences are interpreted and acted upon by the SCP. The actions performed by the SCP are usually the setting or clearing of a bit of an Auxiliary Processor memory location or I/O port. The SCP has access to the control/status records of the AGC Processor and Range Track Processor. Thus, through the SCP, the Workstation can control all three Auxiliary Processors.

The Auxiliary Processor hardware includes a Receive/Transmit (Rx/Tx) Timing Sequencer that generates the global timing signals for the radar. The SCP controls the Rx/Tx Timing Sequencer through a set of I/O Ports. In addition, the Auxiliary Processor hardware also includes a 2048 location frequency/polarization state buffer. This buffer is loaded by SCP commands.

7.0 AUXILIARY PROCESSORS: RANGE TRACK PROCESSOR

The Range Track Processor (RTP) performs the following functions:

- It acts as a high-speed real-time control intermediary for the Workstation.
- It is responsible for both acquisition and track of radar targets.

The Range Track Processor (RTP) in an intermediate level controller implemented as a C language program running in the 80386/7 Auxiliary Processor hardware. The RTP, making use of some special purpose digital circuitry, acts as a high speed control intermediary for the Workstation. The purpose of the RTP is to handle the real-time range tracking tasks that would overly burden the Workstation. Tasks such as range search and range tracking cannot be reliably performed by the Workstation as it responds to asynchronous interrupts. The RTP runs in hardware that is isolated and specially dedicated to the task of high speed control.

The main real-time task performed by the RTP is the real time range tracking of radar targets. The RTP is responsible both for acquisition and track of radar targets. Initially the RTP performs a range search. When the RTP detects a target it automatically switches into range track mode. The RTP is capable of both fixed and variable PRF. Variable PRF is only possible in range track mode. As the target range changes, the RTP adjusts the PRI to keep the target at the maximum unambiguous range.

8.0 AUXILIARY PROCESSORS: AGC-STC PROCESSOR

The AGC/STC Processor performs the following functions:

- It acts as a high-speed real-time control intermediary for the Workstation.
- It automatically adjusts the receiver gain to maintain proper A/D loading; it can be placed in manual gain mode.
- It generates a STC ramp that is added to the gain control voltage, making the target return level independent of range.

A block diagram of the AGC-STC Processor is shown in Figure 9.

The AGC-STC Processor generates the voltage (a_rx_gain) used to control the gain of the 8-channel coherent receiver and the detection subsystem. There are actually two components to a_rx_gain: the STC component and the AGC component.

The STC (sensitivity timing control) component is a time varying voltage which starts increasing at the end of the transmitter pulse duration. The purpose of it is to compensate for the 1/R**4 variation in target return strength that occurs as a function of time. The effect of this is to make target return power (after gain control) independent of range for a fixed target size. The STC voltage can be disabled by the workstation.
Superimposed on the STC component of a_rx_gain is the AGC component. This is a slow varying signal that is generated in the auxiliary processor CPU based on the signals d_sum_copol_i, d_sum_copol_q, d_sum_xpol_i, and d_sum_xpol_q. This signal is D/A converted and added to the STC voltage to generate a_rx_gain. The AGC component is controlled such that the maximum of the magnitude of (d_sum_copol_i, d_sum_copol_q) and (d_sum_xpol_i, d_sum_xpol_q) is at a constant level (64) over a long time average. The AGC component can be manually controlled by the workstation.

The a_rx_gain voltage is sampled at the rising edge of gc_samp and A/D converted to generate d_rx_gain. This signal goes to the data recorder.

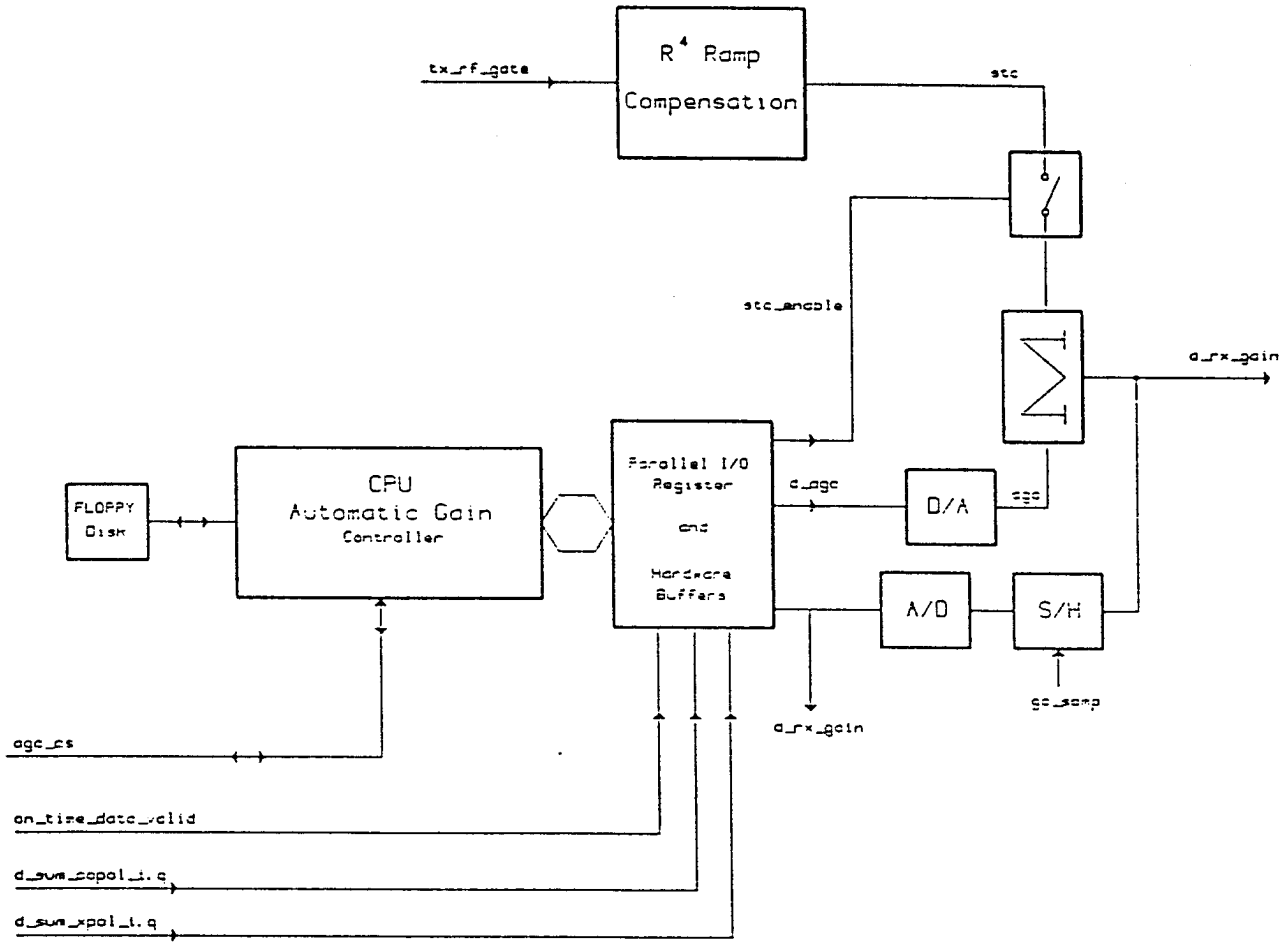

Fig. 7. AGC-STC Processor Block Diagram

2300 Auxiliary Processors
This is the summary level WBS for the effort to specify, design, procure, assemble, produce firmware, and test the system processors, which include the System Control Processor, the AGC Processor, and the Range Track Processor.

2310 Specifications

2320 System Control Processor Design

2330 Range Track Processor Design/Firmware

2340 AGC Processor Design/Firmware

2350 Mechanical Design

2360 Material Procurement/HW Fab & Assy

2370 System Control Processor Test/QA

2380 Range Track Processor Test/QA

2390 AGC Processor Test/QA
Tasks completed. All hardware has been built and firmware has been implemented. Testing referenced in ATP summary to be performed in conjunction with other integration testing.

9.0 ANTENNA SUBSYSTEM

The antenna subsystem performs the following functions:

- It radiates high or medium levels of RF power in either vertical or horizontal polarization, using radiating apertures sized to obtain nominal 3° or 8.5° half power beamwidths, where the power level and beamwidth is selected as a function of target range.

- It simultaneously generates a full complement of monopulse outputs from the target return signal, for both vertical and horizontal polarization, using radiating apertures sized to obtain nominal 3° or 8.5° beamwidths, where the beamwidth selection is changed simultaneously with the transmit antenna.

- It uses separate vertically and horizontally polarized receive antennas to achieve a high level of polarization discrimination in the radar, thereby allowing accurate characterization of target return signal polarization.

The antenna subsystem consists of a set of six antennas, configured to meet the transmit and receive requirements of the Instrumentation Radar System, as well as required waveguide networks and transfer switches. The antennas are mounted on a rigid support frame that interfaces the elevation over azimuth pedestal assembly, and are oriented such that the aggregate cross sectional area is minimized. The antenna complement is characterized as follows:

- One dual polarized 3 degree beamwidth transmit antenna

- Two 3 degree beamwidth receive antennas configured for generation of monopulse outputs (one antenna each oriented for vertical and horizontal polarization, respectively)

- One dual polarized 8.5 degree beamwidth transmit antenna

- Two 8.5 degree beamwidth receive antennas configured for generation of monopulse outputs (one antenna each oriented for vertical and horizontal polarization, respectively)

The 3 degree beamwidth antennas are all implemented using 28 inch diameter parabolic reflector antennas. The 8.5 degree transmit antenna is implemented using a 10 inch diameter parabolic reflector, and the 8.5 degree beamwidth receive antennas are implemented using pyramidal horn assemblies. The dual polarized transmit antennas use a square feed aperture in conjunction with an orthomode transducer and polarization switch to allow selection of either vertical or horizontal polarization on either a continuous, frame by frame, or pulse to pulse basis. The receive antennas are equipped with a four hybrid monopulse comparator network for

generation of the sum(reference), azimuth error, elevation error, and diagonal error signals required for tracking and data collection. The comparators are implemented in waveguide, and are located immediately adjacent to the horn/feed assemblies in order to minimize amplitude and phase balance errors prior to the comparator. Phase matched waveguide runs are used to route the monopulse signals into the RF enclosure where the receiver front end hardware resides for subsequent amplification and downconversion.

2400 Antennas/Transmission Lines
This is the summary level WBS for the effort to specify, design, procure, fabricate, assemble, and test the narrowbeam and widebeam antenna feeds and reflectors and the RF transmission lines.

2410 Fabricate & Inspect Reflectors
Task completed. All reflectors have been inspected for mechanical integrity and tested for surface accuracy.

2420 Fabricate and Inspect Feed Horns & Preliminary Testing
All feeds have been fabricated, and testing is substantially completed. The only remaining task is to perform additional impedance tuning on the two monopulse feed horn assemblies for the narrowbeam antennas and test these feeds.

2430 Fabricate and Inspect Antenna Frame
Task completed. The antenna frame has been installed on the pedestal, and all antennas have been mounted to assure proper interface to the frame. The camera assembly has also been mounted on the antenna frame.

2440 Lay out Waveguide Runs & Fabricate Final Waveguide & Cables
Design and procure parts for waveguide run from antenna positioner to transmitter rack. Design and procure parts for waveguide interconnections on antenna positioner. Design routing of receiver cables on antenna positioner assembly.

2450 Mount Antenna Frame on Pedestal
Task completed. Pedestal has been exercised with entire antenna complement mounted.

2460 Mount Antennas on Frame
Install feeds in reflectors, which are already mounted onto the frame. Install broadbeam horn assemblies onto the frame.

2470 Interconnect Waveguide
Assemble all waveguide in place and test for electrical/physical integrity. Install receiver cables in final configuration. Test all cabling/waveguide while moving antenna positioner through limits of motion.

2480 Take Antenna Patterns
Set up for antenna pattern testing of all antennas (mounted on antenna frame/positioner) and collect data per the ATP summary.

2500 Material & Mechanical Engineering Support

This WBS item was added to provide one WBS for material remaining to be acquired as opposed to putting material with its related subsystems. Since there is so little material left to purchase, it is more convenient to address it in one spot. The total material cost is $768,205 of which only $7500 is left to purchase.

In addition, the bulk of the mechanical engineering work has been accomplished and was charged to specific tasks. What is remaining is mechanical engineering support for final assembly, integration, and testing as the need arises. For this reason, we have put all of the ME effort in this WBS item.

10.0 POSITIONER SUBSYSTEM

The positioner subsystem performs the following functions:

- It uses the normalized monopulse error signals provided by the Az/El Track Processor to close a servo loop and generate drive signals for the dual axis pedestal to automatically track a target
- It provides a mechanism for the operator to point the antennas at a coordinate in a pre-planned flight path for acquisition purposes
- It allows the operator to manually control the pointing direction of the antenna

The positioner subsystem consists of a dual axis elevation over azimuth pedestal with associated drive motors and servoamplifiers, and a positioner controller that interfaces 1) the workstation for the purpose of selection of controller operating mode and 2) the azimuth/elevation tracking processor for the purpose of reading the normalized monopulse error signals and returning angle data.

The pedestal is a fully MIL-qualified unit (ref: AB1303/TMQ¬31) that uses aluminum construction. Approximately 80 of these units have been delivered to the Army. The unit uses spur gear drive assemblies in both axes, with adjustable backlash. The drive shafts are supported by four point contact bearings. Each axis has the same drive motor and data package consisting of dual synchros (coarse and fine). The drive motor for each axis is a permanent magnet DC servomotor with integral tachometer.

The pedestal controller consists of a standard set of boards integrated into a package capable of providing the required modes of operation, servo performance, and data interfaces. The modes of operation include:

- STANDBY: The pedestal is idle until another mode of operation is selected
- DESIGNATE: The pedestal may be commanded over the IEEE bus to go to an externally commanded position
- AUTOTRACK: The pedestal uses the normalized monopulse error signals supplied by the AZ/EL track processor to close the servo loop and perform automatic target tracking using a Type I modified position loop with internal tach loop.
- MANUAL (RATE): The pedestal is moved using a rate control implemented in a joystick.

The positioner controller modes of operation will be automatically selected by the workstation over the IEEE bus based on the selected mode of operation for the radar.

The position servo loop is adjustable to accommodate varying loads as well as different dynamic requirements. The required minimum velocity constants to achieve the dynamic tracking error levels budgeted for the pedestal and servo loop are approximately 150 and 50 for azimuth and elevation, respectively. The servoloop constant in the IRS unit will be adjustable to achieve velocity constants of up to 300. The output angle data is routed over a parallel interface to the AZ/EL track processor for conversion to balanced TTL, then to the data recorder subsystem where it is multiplexed onto one of the digital recorder tracks, and is also sent to the workstation for real time display.

2600 Pedestal/Controller
This is the summary level WBS for the effort to specify, procure, and test the positioning subsystem.

2610 Procure, Receive & Inspect Pedestal/Controller
This task initially covered writing the specification for the IRS positioning subsystem, selecting the vendor and supporting him in his efforts, witnessing vendor ATP, and receiving and inspecting the pedestal/controller at FR. At this time, all of these subtasks tasks have been completed. The selected vendor was Rotating Precision Mechanisms (RPM). FR supported the vendor in his design of interfaces to the antenna and to the deck of the trailer, as well as with required electrical interfaces from the controller to the positioner. FR visited the vendor's facility for a technical exchange meeting while work was in process and made another trip to witness final acceptance tests.

2620 Interface with Workstation
Task completed. The primary function of the workstation interface is for selection and control of the positioner controller mode of operation (joystick, designate, or autotrack).

2630 Mount on Trailer/Rack/Cable
Task completed. The pedestal now resides in its permanent location on the rear porch of the trailer.

2640 Pedestal Checkout
Task completed. The pedestal has been thoroughly exercised after being mounted onto the trailer assembly, and tested for proper velocity and limits.

11.0 VIDEO SUBSYSTEM

The Video Subsystem views the radar target with a video camera and monitor, records the video, and annotates it with IRIG and system inputs. Its specific functions are as follows:

- It views the target through a video camera mounted on the Pedestal Subassembly, and allows the user to see it from a monitor inside the trailer.
- It records the video on a VCR that is inside the trailer.
- It generates IRIG timing signals, displays them on the monitor, records them on the VCR, and sends them to the Workstation.
- It annotates the video on the monitor with test information and angle data.

The video subsystem consists of five commercial/industrial grade components: the camera, IRIG generator/translator, annotator, video recorder (VCR), and monitor. The video signals are monochrome, follow the RS-170 standard, and are compatible with NTSC.

The camera, manufactured by COHU electronics, is designed for use on outdoor mobile and tracking installations and is contained in an environment proof housing. It includes a zoom lens, remotely controlled at the IRS workstation.

The IRIG generator/translator reads IRIG A, B, E, G, and H signals and can also generate its own IRIG time from a sync or start pulse and the 10 MHz reference signal from the synthesizer/LO subsystem. The time output signals are in three forms: IRIG B data for the data recorder and a VCR audio channel, BCD digital data for the annotator, and RS-232 data for the workstation. The time resolution is 1 millisecond.

The annotator derives sync from the camera video signal, and superimposes information on the video signal. This information is IRIG time on one caption, and 32 alphanumeric characters received from the workstation RS-232 bus on another caption. This line is AZ/EL data and the test number as entered by the operator. Crosshairs are also added to the video signal.

The VCR records and plays back the video signal and two audio channels. This is an industrial or broadcast grade super-VHS unit which has 400 lines per field resolution, as set by the S-VHS standard. This unit limits the video subsystem resolution.

The monitor is a 15 inch rack mount unit. It displays live or prerecorded video. The block diagram of the subsystem is shown in Figure 11.

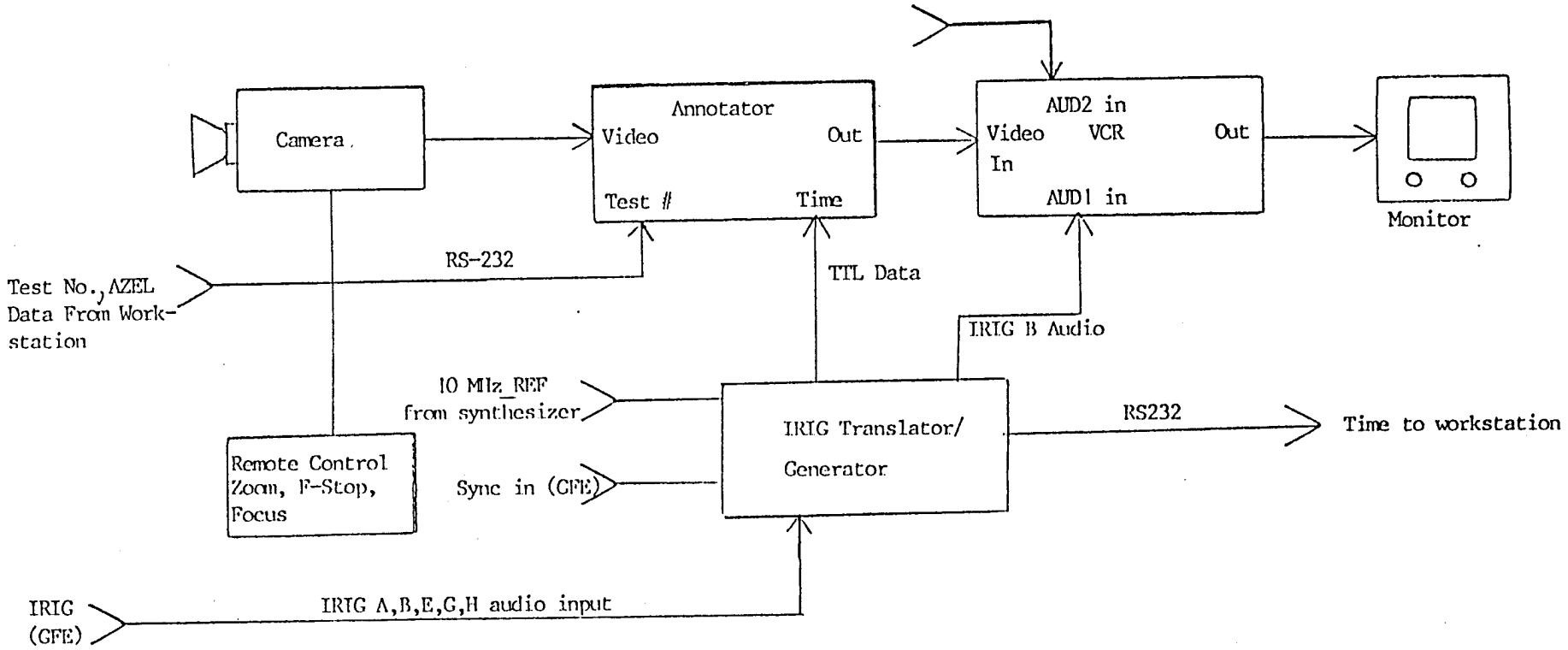

Fig. 8. Video Subsystem Block Diagram

2700 Camera/Recorder Subsystem
This is the summary level for the effort to specify, procure, inspect, install, and test the video camera and video recorder.

2710 Mount Camera on Antenna Frame & Cable
Task completed. Camera has been tested for proper functionality while mounted on the antenna frame. Control of the zoom lens and proper display on the monitor inside the trailer has been demonstrated while the pedestal is in motion.

2720 Mount Video Equipment in Rack & Cable
Task completed. Tests have been performed as described in 2710 above.

2730 Integrate with Workstation & Test
Task completed.

12.0 TRAILER

The trailer performs the following functions in the IRS:

- It provides a stable platform for the tracking antenna/ positioner assembly, which is an important element in minimizing tracking error.
- It provides a temperature controlled and weatherproof environment for the system electronics and operators.
- It allows the system to be conveniently transported and set up at different measurement sites.
- It provides prime power for the entire IRS.

The trailer is a mobile, towable unit comprised of an enclosed area and an open "flatbed" area. Figure 11 defines the plan dimensions and layout of the trailer installed equipment. A separate portable generator provides electric power.

At the aft (open) end of the trailer, the radar antennas are mounted on a dual axis pedestal. Within the closed section are the equipments and facilities for operating the system. Heating, cooling and lighting are provided to accommodate personnel. Steps and a side door allow access. A system of (6) manual jacks level the trailer. A weather station, mounted on an outside mast provides wind speed, wind direction, temperature and barometric pressure, with readouts available inside the trailer enclosure. The enclosed structure is EMI/RFI shielded, and power lines are filtered. A door at the rear of the closed area opens to the flatbed area. Removable railings edge the three open sides. A safety "disable" switch protects personnel from working near an operating pedestal or transmitter.

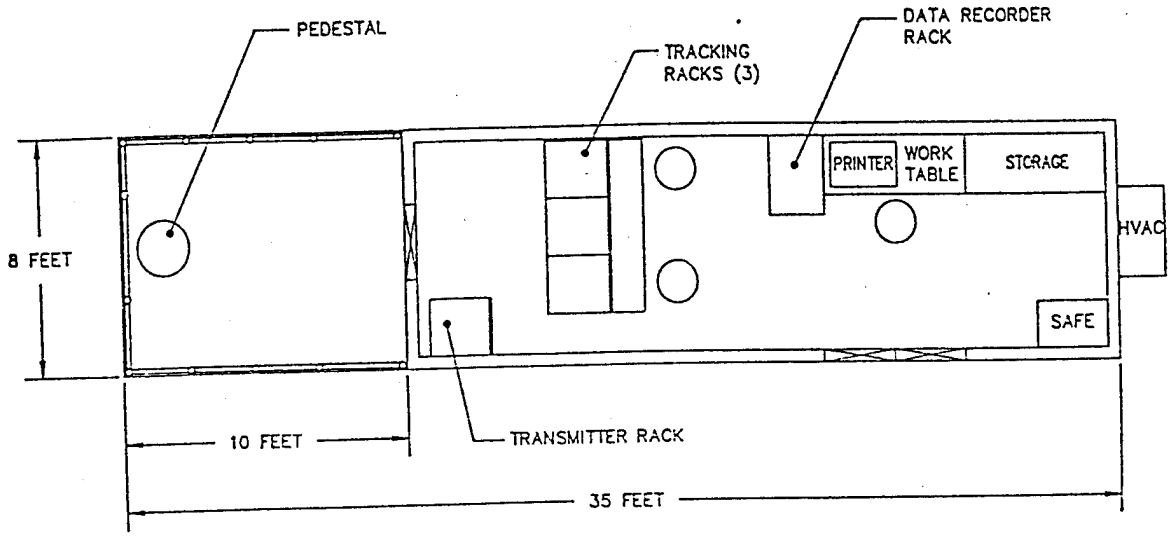

Fig. 9. Trailer Layout

2800 Trailer

This is the summary level for the effort to specify the physical characteristics of the trailer, design the electrical and environmental systems for the trailer, select and support a trailer vendor, receive and inspect the trailer, bring power to the trailer, and install and test the trailer accessories. The trailer was built by Williams Mobile Offices to FR specifications and delivered to FR's facilities. Power was run to the trailer and the electrical and HVAC systems have been checked out and are functioning. All of the effort for this subsystem is complete except as noted below.

2810 Trailer Inspection

Task completed. The trailer construction was inspected in progress at the factory in Indiana, and again upon completion.

2820 Support Vendor Corrective Actions

Task completed. Several minor repairs were made by the vendor at the FR facility after delivery of the trailer.

2830 Bring Power to Trailer and Test HVAC System

Task completed. The power and HVAC systems have been cycled numerous times since delivery of the trailer to the FR facility.

2840 Install & Test Trailer Accessories

Install wiring for interlocks, safety lights and emergency power shutdown, and test. Install proper outlet type required by transmitter.

2900 Calibration Target

This is the summary level for the effort to design, procure, assemble and test a fixed target to be used for calibrating the IRS. To date, the design of the fixed target has been started. The effort needed to complete this subassembly is described below.

2910 Design of Fixed Target

Complete design of mechanical support/mount for selected dihedral target.

2920 Fabricate and Test

Procure standard dihedral target and fabricate permanent mounting frame. Check mechanical integrity of completed assembly and perform electrical test of assembly to ensure contributions from mount and target mount/interactions are acceptably small.

13.0 WORKSTATION

The workstation performs the following functions:

- It runs the IRS operating software implemented as a C language program running in the 80386/7 Workstation hardware.
- It is responsible for low-speed control of all major IRS subsystems.
- It supports user interfaces through two displays, a keyboard, mouse, and joystick.
- It displays samples of real time data being acquired.
- It performs automatic internal calibration of IRS receivers.

The Instrumentation Radar System contains many specialized processors, each of which needs a unique set of parameters for a particular test scenario. Rather than having a very rigid structure, where parameters are fixed in a PROM, many of these parameters will be operator selected in order to allow the operator maximum flexibility in tailoring the system for a wide range of measurement programs. The role of the workstation PC is to be an operator interface to the rest of the system, feeding specialized processors the required information. The PC will have no real time functions, only set up and subsampling requirements; i.e., status display, periodic monitoring of data during collection, and post processing data display.

The system will allow maximum operator flexibility within equipment performance constraints, and will not bias operator test menu set-up in general. That is, it will allow the operator to request parameter combinations that, under normal circumstances, would be deemed to be incompatible, in order to allow for the possibility that under special test measurement conditions such combinations may actually be desirable. Only combinations that would be detrimental to system hardware will be disallowed. Configuration files may be loaded into the system for parameter combinations that are utilized often.

Software will be run on the workstation, and it will interface with external equipment as specified in the System Interface Document, DWG. NO. IC050040-01.

14.0 OSCILLOSCOPE SUBSYSTEM

The Oscilloscope Subsystem provides an A-scope display, timing information, or analog I/Q display, on two oscilloscopes. The specific functions of the Oscilloscope Subsystem are:

- It displays the magnitude of the co-polarized and cross-polarized signal for any one of four comparator outputs.
- It displays the transmit and receive timing pulses.
- It displays the I and Q baseband of either the co-polarized or cross-polarized signal for the same comparator output that is shown on the A-scope display.

The oscilloscope subsystem shown in Figure 8 allows the operator to observe an A-scope display or I/Q signal pair for a selected received channel. A four-channel oscilloscope serves as the A-scope display. In operation, two traces will show the amplitude of a particular channel versus range (xpol and copol), while the remaining two traces will display timing signals.

The analog inputs to the oscilloscope subsystem consist of 16 baseband signals from the detector subsystem. These are the I/Q pairs of the four received xpol and copol channels (sum, daz, del, ddx). The subsystem produces the xpol and copol log magnitude ($I^2 + Q^2$) of a particular channel for use in the A-scope display. Through use of a manual rotary switch, the system allows the operator to choose the desired channel. The manual switch controls a bank of high bandwidth switches which connect the selected channel's copol and xpol I/Q signals to the log magnitude circuitry. These same signals are also directed to a second group of video bandwidth switches which allow the operator to determine whether xpol I/Q or copol I/Q signals are displayed on the lissajous figure. A second rotary switch controls the selection. The analog outputs are short-circuit protected.

In addition to the xpol and copol log magnitude, the four-channel oscilloscope is able to show the tx_rf_gate and the on_time_samp signals which are derived from balanced digital inputs. The on_time_samp pulse can be used as an aid to the operator in locating the returned target pulse. The tx_rf_gate is used as the external trigger for both oscilloscopes, but it is needed for the two-channel oscilloscope only when the I/Q signals wish to be seen independently. Both digital signals are short circuit protected.

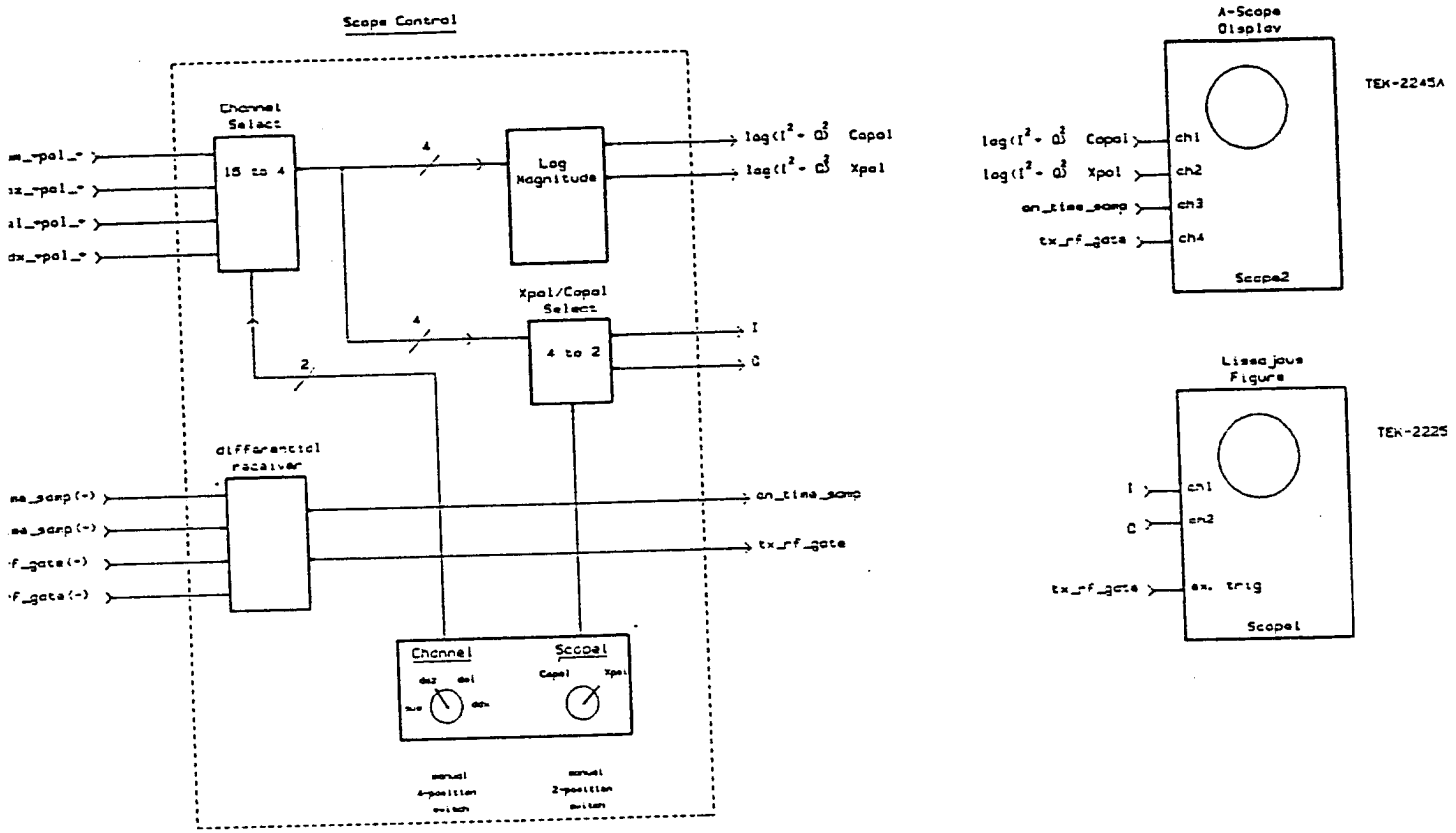

Fig. 10. Oscilloscope Subsystem

2A00 Workstation
This WBS item is the summary level for the effort to specify, procure materials for, fabricate, assemble and test the operator workstation with its racks and associated accessories. Included in this effort are the computers, scope displays, scope control assembly, and the joystick box, among others.

2A10 Complete Workstation Wiring
Complete custom wiring inside processor enclosure.

2A20 Set up Directories & Load System Software
Remove all intermediate, development, and outdated files; leave all system software in final directories.

2A30 Set up Directories & Load System Firmware
Load final firmware into system. Remove temporary hard drive being used with display processor and burn PROM for display processor software and install.

2A40 Complete Scope Subsystem
Finish debugging of scope control board. Complete assembly of scope control box and test.

2A50 Workstation Integration Testing
Test workstation in final hardware/software configuration.

15.0 DATA RECORDER SUBSYSTEM

The Data Recorder Subsystem converts parallel digital data from several subsystems to high speed serial data, then records it on a multichannel tape recorder. It also plays back the data from the tape recorder to the workstation via a serial/parallel conversion, or it picks off some real-time data that is being recorded and sends it to the workstation. The particular functions of the Data Recorder Subsystem are as follows:

- It takes parallel digital radar data from the Detection Subsystem as well as AGC data, range and angle track data, transmit power data, and system status data from other subsystems and converts it to serial digital data.
- It records the converted data on the digital tape recorder in serial form.
- It provides real-time playback of subsampled parallel data streams to the Workstation while the conversion and recording process proceeds.
- It plays back the serial data from the digital tape recorder.
- It converts the serial playback data to parallel data and sends it to the Workstation.

The role of the Data Recorder Subsystem is to receive, format, and then record all relevant test data on magnetic media for subsequent analysis. All data is sampled on the rising edge of the data_valid clock whose frequency matches that of the variable prf_clock rate. Through the workstation, the operator will have a limited ability to select sampled data for both real-time and post-acquisition playback display.

Figure 7 shows the Data Recorder Subsystem Block Diagram. The Digital Tape Transport (DTR), Digital Record Unit (DRU), and Digital Playback Unit (DPU) represent the Honeywell model HD-101e data storage system. It is remote controlled via an IEEE-488 interface to the workstation and is configured for 3 analog and 25 digital data tracks (note: 2 digital tracks required for parity overhead).

The remaining subsystem components depict the Data Conditioner Unit. This is a FR designed cardrack consisting of 10 printed circuit boards. The dashed lines outline the 5 unique board types as described below.

(1) **CONTROL BOARD:** [Qty: 1] Communicates with the workstation to produce data bus select/enable signals. Receives data_valid clock which is synchronized to its own bit rate clock to produce timing signals for latching data and format conversion.

(2) **SINGLE PORT RECORD BOARD:** [Qty: 1] Receives Azimuth, Elevation, Range Delay, and Workstation Record data. Conversion from parallel to serial format is performed before multiplexing all data onto a single recorder track. Allows operator to select any 1-of-4 data words for subsampled real-time playback display.

(3) **DUAL PORT RECORD BOARD:** [Qty: 6] Receives all I/Q, AGC, System Status, and Forward Power data. Conversion from parallel to serial format is performed before being stored on 21 recorder tracks. Allows operator to select any 2-of-11 data words for subsampled real-time playback display.

(4) **SINGLE PORT PLAYBACK BOARD:** [Qty: 1] Executes the inverse of board type 2. Conversion from serial to parallel format is performed with synchronization to demultiplex the information back to 4 data words. Allows operator to select any 1-of-4 data words for subsampled post-acquisition playback display.

(5) **DUAL PORT PLAYBACK BOARD:** [Qty: 1] Executes the inverse of board type 3. Allows the operator to select any 2-of-11 data words for subsampled post-acquisition playback display before conversion from serial to parallel format is performed.

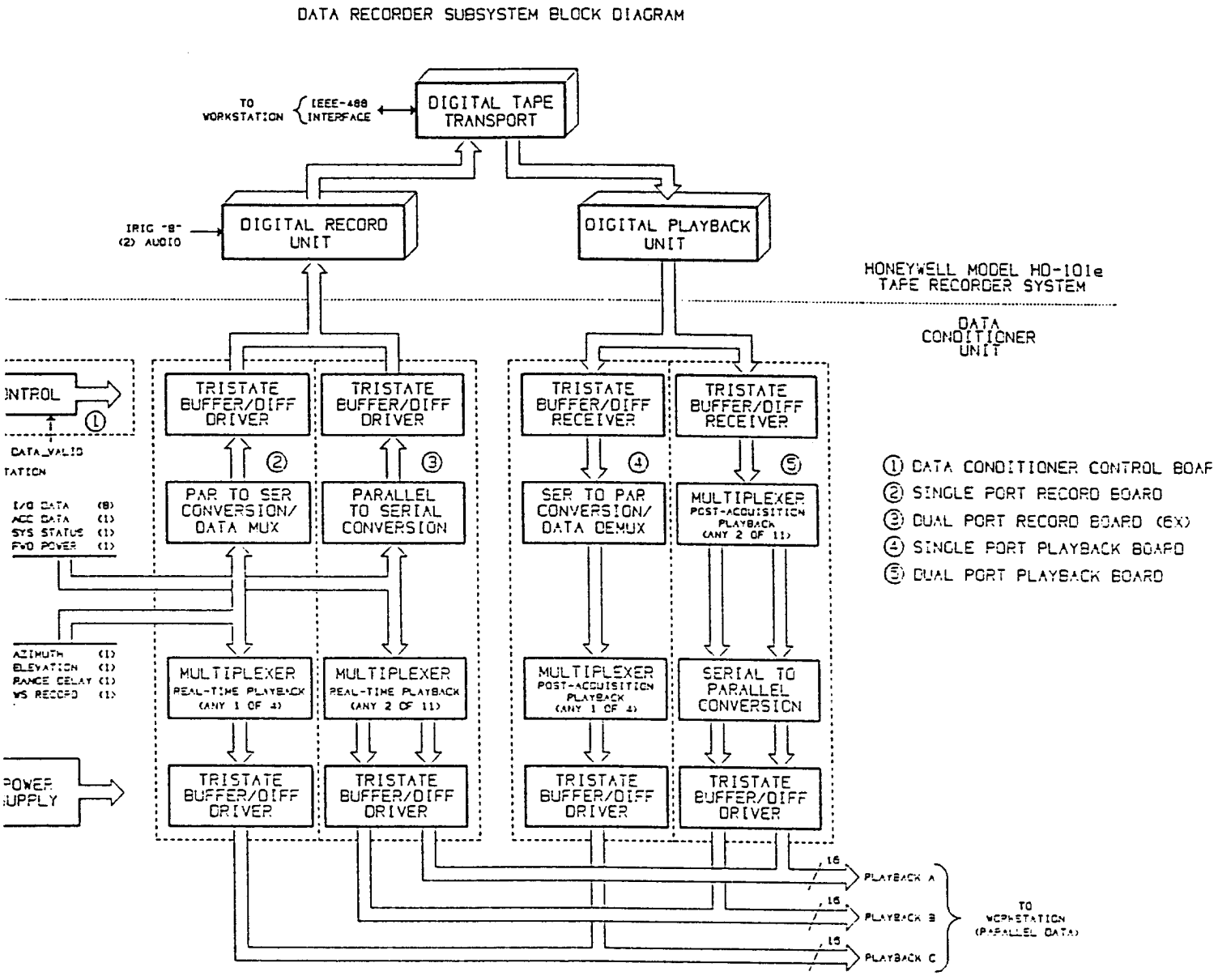

Fig. 11. Data Recorder Subsystem Block Diagram

2B00 Data Recorder Subsystem
This is the summary level WBS for the effort to specify, procure, and test a high speed digital data recorder, and to design, build, and test a data conditioner subassembly to interface the data recorder to the custom IRS data collection hardware. This effort is completed except as noted below.

2B10 Test Honeywell System
Task completed. Honeywell performed a standard test on the unit at the factory, as well as additional testing after installation in the trailer at the FR facility to verify functionality and performance levels.

2B20 Data Conditioner Assembly & Test
Finish assembly of back panel and recheck unit. Complete integration into recorder rack. At this point, all boards in the unit have been tested in the backplane. The only remaining wiring to be verified are the connections to the unit back panel.

2B30 Complete Audio Mux Board Layout; Fab & Test
Complete automated layout of board; procure PC board, populate, and test. Integrate into Data Conditioner unit.

2C00 Interconnection Subsystem
This is the summary level WBS for the effort to design and document the interconnections between all of the subsystems comprising the IRS.

2C10 Document Interconnections
Complete documentation of all subsystem interconnections; task is substantially complete.

2D00 Integration Cabling
This is the summary level WBS for the effort to specify, document, procure, fabricate, and test the cables needed to integrate the IRS system.

2D10 Document Cabling
Complete documentation of physical cable assemblies; task is substantially complete.

2D20 Build & Test Cables
Fabricate remaining interconnecting cable assemblies between enclosures in trailer and test for electrical and physical integrity.

2D30 Integrate Cables into Trailer
Install and dress cables in tracking racks.

16.0 AZ/EL TRACK PROCESSOR

The Az/El Track Processor performs the following functions:

- It generates and properly scales the normalized monopulse error signals required by the positioner controller to close the servo loop during automatic tracking
- It compensates for the difference in relative phase in the monopulse channels between the broadbeam and narrowbeam antennas
- It compensates for the error signal slope differential between the narrowbeam and broadbeam antenna

A block diagram of the AZ/EL Track Processor is shown in Figure 10.

This subsystem generates the two error voltages, az_error and el_error, used to drive the positioner controller.

Three signals from the Detection Subsystem, if2_sum_copol_track, if2_daz_copol_track, and if2_del_copol_track pass through gain control amplifiers. The gain control amplifiers are all controlled by the same control voltage which works to make the on-time sampled amplitude of the sum signal a constant level on the average.

The sum signal is then mixed with the daz and the del signals to generate two baseband signals. The baseband signals are sampled and held on the rising edge of on_time_samp, giving az_error and el_error. The magnitude and sign of the error signals indicate how far off target the antennas are pointing.

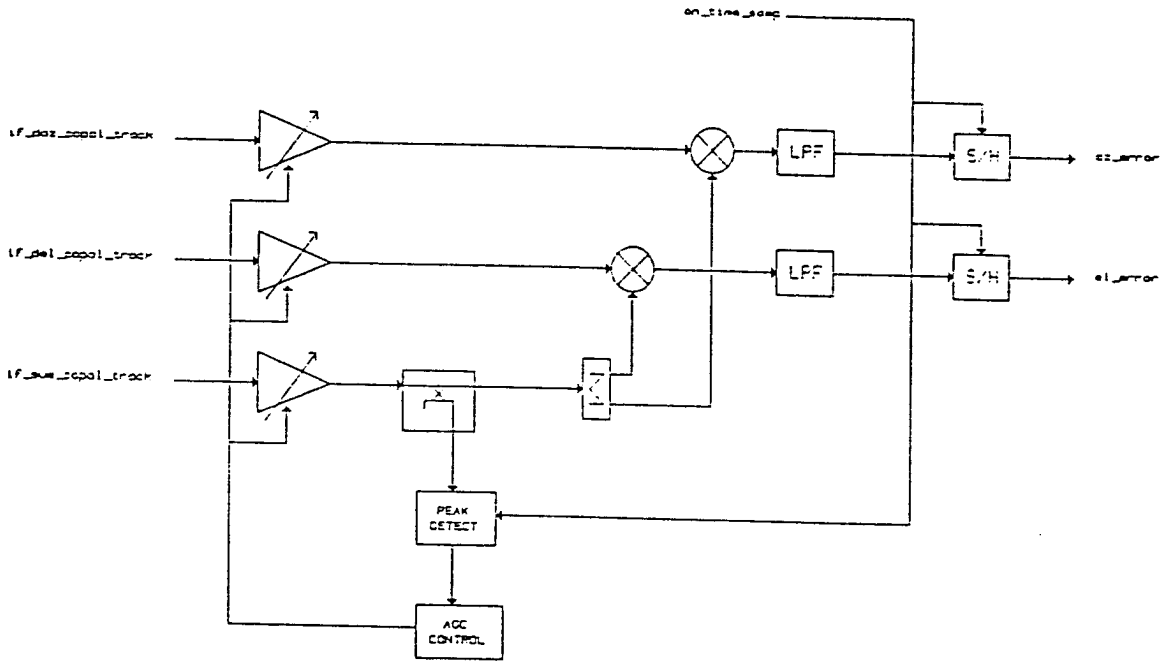

Fig. 12. AZ/EL Track Processor Block Diagram

2E00 AZ/EL Preprocessor
This is the summary level WBS for the effort to specify, design, procure, fabricate, assemble, and test the AZ/EL Preprocessor assembly.

2E10 Test Processor Boards
Tasks completed. This includes testing of the control board, data boards, variable attenuator board, error detector board, and sample/hold board.

2E20 Assemble Processor Box
Task completed.

2E30 Rack and Cable
Task completed.

2E40 Integration and Test
Perform tests per ATP summary.

3000 Software
This is the summary level WBS for the effort to specify, design, code, and test all the software required for the IRS system operator interface and workstation displays.

3100 Complete Code and Unit Test
Task completed. The software was coded in accordance with a software requirements specification and a software design document.

3200 Software Integration Testing
Complete modifications required to correct deficiencies identified during previous software integration tests/test plan execution.

3300 Formal Software Testing
Conduct formal software testing per the approved software test plan.

3400 Update Software Documentation
Document corrections resulting from the modifications executed in task 3200.

3500 Software QA
Perform software QA audit, configuration control, and other functions per FR internal procedure.

3600 Produce Software End Item
Prepare final software item for integration into the system in its final configuration, and for delivery on appropriate media.

4000 System Integration
This is the summary level WBS for the efforts to integrate the various hardware subsystems and the system software into a functioning IRS.

4100 Verification of Positioner Tracking Capability
Task Completed. An ATP was performed according to an approved plan at the RPM facility in Northridge, CA.

4200 Receiver/Transmitter Integration Testing
Perform tests per the ATP summary.

4300 Workstation/Data Recorder Integration Testing
Integrate workstation/data recorder and debug the interface between the subsystems. Perform tests per the ATP summary.

4400 System Level Static Data Collection
Perform tests per the ATP summary.

4500 System Level Dynamic Data Collection
Perform tests per the ATP summary.

5000 Factory Acceptance Testing
Allows time for official demonstrations of subsystem level, integration, and system level tests to customer. Assumes subsystem and integration tests are performed as they occur in the process of integrating and testing the radar in order to maximize efficiency.

6000 Site Activation
Pack and ship radar to NWC, China Lake and assist in set up and checkout of system.

7000 Documentation
This is the summary level WBS for the efforts to fully document the deliverable IRS.

7100 Drawings
Complete drawing package.

7200 Configuration Management
Maintain configuration management in accordance with the approved plan.

7300 Manuals
Prepare an operations and maintenance manual in accordance with the CDRL and using Data Item Description (DID) DI-M-30423 as a guide.

8000 Program Management
This is the summary level WBS for the project's management efforts.

8100 Program Control/Technical Management
Includes time for the program manager and an administrator to perform cost and schedule control functions, and for the project engineer to oversee the technical progress of the program.

8200 Meetings and Reviews
Time for attendance of weekly in-house project status meetings and reviews with the customer.

9000 CDRL Items **
This is the summary level WBS for the efforts to produce the remaining data and documentation required by the Contract Data Requirements List.

9110 A003, Safety Assessment Report
Prepare a safety assessment report in accordance with the CDRL and using DID DI-SAFT-80102 as a guide.

9120 A005, Acceptance Test Plan
Prepare an Acceptance Test Plan in accordance with the CDRL and using DID DI-T-5204 as a guide. The test plan will be based on the ATP summary submitted with the April 4 quote.

9130 A007, Progress Report
Prepare monthly progress reports in accordance with the CDRL and using DID DI-MGMT-80227 as a guide.

9140 A008, Minutes
Prepare minutes of conferences in accordance with the CDRL and using DID DI-A-7089 as a guide.

9150 A009, Engineering Drawings
Prepare copies of Engineering Drawings in accordance with the CDRL.

9160 A00A, Acceptance Test Report
Prepare and submit results of testing performed under the Acceptance Test Plan in accordance with the CDRL, using the executed data sheets from the Acceptance Test Plan as the primary substance of the report, and using DID DI-T-2072 as a guide.

9170 A00B, Contract Summary Report
Prepare and submit a report detailing efforts performed under the contract in accordance with the CDRL and using DID DI-ADMN-80447 as a guide.

9180 A00C, Operation and Maintenance Manual
Prepare O&M Manual drafted under task 7300 for formal submittal.

9190 A00K, Software Test Report
Prepare and submit results of the formal software testing in accordance with the CDRL and using DID DI-MCCR-80017 as a guide. The executed data sheets from the approved software test plan will form the primary substance of the report.

91A0 A00L, Computer SW
Deliver software to the government on appropriate media in accordance with the CDRL using DID DI-H-5545 as a guide.

91B0 A00P, Engineering Change Procedures
Prepare ECP's for submittal to the government in accordance with the approved Configuration Management Plan, using FR in-house ECP documentation procedures.

91C0 A00Q, Agenda

Prepare agenda for formal reviews in accordance with the CDRL.
** The following CDRL items have been submitted and approved; therefore, they are not addressed in our proposal or this document.

A001, A002, A004, A00D, A00E, A00F, A00G, A00H, A00J, AOOM, AOON, A00R